REMARKS

In response to the Office Action mailed July 3, 2003, Applicant has amended the application as above. No new matter is added by the amendments as discussed below. Applicant respectfully requests the entry of the amendments and reconsideration of the application in view of the amendments and the remarks set forth below.

Discussion of Claim Amendments

Claims 2, 10, 12, 18, 27 and 30 have been amended. Upon the entry of the amendments, Claims 1-31 are pending in this application. The amendments to Claims 2, 27 and 30 are merely to rewrite the claims in independent form. The amendments to Claims 10, 12 and 18 are merely to correct technical errors. Thus, the claim amendments do not narrow the scope of protection. Also, no new matter is added by the amendments. Applicant respectfully requests the entry of the amendments.

Discussion of Drawing Objection

The drawings have been objected to by the Draftsperson. In reply, Applicant submits herewith a set of formal drawings that have resolved all of the issues addressed in the Notice of Draftsperson's Patent Drawing Review. Withdrawal of the objection is respectfully requested.

Discussion of Claims 2-23, 27 and 30-31

The Examiner has indicated that Claims 2-23, 27 and 30-31 would be allowable if rewritten in independent form. Claims 2, 27 and 30 have been rewritten in independent form to include all of the limitations of the base claim and any intervening claims. Claims 3-23 and 31 depend from base Claim 2 or 30. Thus, Claims 2-23, 27 and 30-31 are allowable over the cited references.

Discussion of Claim Rejections Under 35 U.S.C. § 102(b)

The Examiner has rejected Claim 1 under 35 U.S.C. § 102(b) as being anticipated by Yeh, et al. entitled "OPERAS in DSP CAD Environment." Claim 1 is not anticipated by the Yeh reference as discussed below.

Standard of Anticipation

"For a prior art reference to anticipate a claim under 35 U.S.C. § 102, every element of the claimed invention must be identically shown in a single reference." *Diversitech Corp. v. Century Steps, Inc.*, 850 F.ed 675, 677, 7 USPQ 2d 1315, 1317 (Fed. Cir. 1988).

Discussion of Patentability of Claim 1

Claim 1 recites, among other things, representing a behavioral description of said system as a first set of objects with a first set of relations therebetween, and refining said behavioral description into an implementable description of said system, said implementable description being represented as a second set of objects with a second set of relations therebetween. However, the Yeh reference does not show the above-recited features as discussed below.

1. Yeh Does Not Show Representing a Behavioral Description

As is used in Claim 1, the term 'behavioral' means a structure-free, high-level description wherein the desired behavior of the system is substantiated in a formal and abstract way. In one embodiment of the invention, the behavioral description can include a data vector model. It must be emphasized, however, that that the invention is not limited to using this model. In contrast, Yeh describes a CAD environment for providing algorithmic and hardware architecture optimization using a description defining hardware structure (page 130, abstract). The examples provided in Yeh all clearly show structural information. Referring to page 132, section 3.2, second paragraph, the study of structure, such as gate and macrocell level structures are described.

The Examiner asserts that Yeh defines a behavioral description being represented as objects at page 131, section 2.1, fourth paragraph. Applicant respectfully disagrees with the Examiner. Yeh at best discloses, in the same paragraph, that DSP designers often write system behavioral models in a general purpose language such as C. However, as discussed above, Yeh is directed to algorithmic and *hardware architecture optimization* using a description defining *hardware structure*. Therefore, Yeh does not show representing a behavioral description of said system as a first set of objects with a first set of relations therebetween.

2. Yeh Does Not Show Refining the Behavioral Description Into an Implementable Description

Yeh discloses a single way of describing a system (nets and modules) (page 132, section 3.1, first paragraph). In contrast, the clamed invention refines the behavioral description, which is represented as a first set of objects, into an implementable description being represented as a second set of objects. One embodiment of the claimed invention utilizes refinements which achieves a shift from a first type of representation (a first set of objects) to a second type of representation (a second set of objects) that is different from the first type. In one embodiment of the invention, the first set of objects is a data-vector model and/or a data-flow model, and the second set of objects is a signal flow graph (SFG) data structure. *See* column 5, lines 9-13, or claims 9 and 10 of the parent patent (U.S. Patent No. 6,606,588), which has been incorporated by reference into this application.

In addition, in the Notice of Allowability dated April 25, 2002, for the parent application (Application No. 09/237,549), the Examiner confirmed that Yeh fails to teach, suggest or render obvious "generation of an implementable description of a system from the behavior description of said system utilizing transformation and/or refinements to shift between the description types." Claim 1 includes a similar limitation, which is "*refining* said behavioral description *into an implementable description* of said system, said implementable description being represented as a second set of objects with a second set of relations therebetween." Therefore, Applicant respectfully submits that Yeh does not show the refining said behavioral description into an implementable description of said system recited in Claim 1.

3. Summary

As discussed above, Yeh shows neither the use of a behavioral description nor describes refining the behavioral description into an implementable description recited in Claim 1. Thus, the Yeh reference does not show every element of the claimed invention. Applicant respectfully submits that Yeh does not anticipate Claim 1. Furthermore, since Yeh does not teach or suggest the recited features, Claim 1 would not have been made obvious over the reference, either. Therefore Claim 1 is patentable over the Yeh reference. Withdrawal of the rejection is respectfully requested.

Discussion of Claim Rejections Under 35 U.S.C. § 103(a)

The Examiner has rejected Claims 24-26 and 28-29 under 35 U.S.C. § 103 (a) as being unpatentable over Yeh in view of Rostoker, et al. (U.S. Patent No. 5,544,067). However, Claims 24-26 and 28-29 are patentable over the cited references as discussed below.

Standard of *Prima facie* Obviousness

In order to provide a *prima facie* showing of obviousness under 35 U.S.C. § 103, all the claim limitations must be taught or suggested by the prior art. *See, e.g., In re Royka,* 490 F. 2d 981, 180 U.S.P.Q. 580 (CCPA 1974); MPEP 2143.03.

No *Prima facie* Case of Obviousness

Independent Claim 24 recites, among other things, transforming the behavioral register-transfer level (RTL) design description into an object hierarchy and creating an object that comprises a method capable of transforming said object hierarchy into a second object hierarchy that describes said target hardware component. However, neither Yeh nor Rostoker teaches or suggests the above-recited features.

As discussed above in connection with patentability of Claim 1, Yeh only discloses a single way of describing a system (nets and modules). Thus, Yeh does not disclose or teach transforming the RTL level design description into an object hierarchy. Similarly, Yeh does not disclose or teach creating an object that comprises a method capable of *transforming said object hierarchy into a second object hierarchy* that describes said target hardware component. Thus, Yeh does not suggest or teach all of the claim limitations of Claim 24.

Rostoker neither teaches nor suggests the above cited features. The Rostoker reference discloses that the resulting resister-transfer level (RTL) description is simulated in a block (1216), and minimized in a block (1218). The RTL description design consists of synthesizable parts (combinational logic, registers, flip-flops) and non-synthesizable parts (pre-designed blocks). Rostoker also discloses that the RTL design of the synthesizable parts is optimized in a block (1224) to produce a gate-level net list (1226) (column 13, lines 44-58; Figure 12). That is, the Rostoker system at best produces the gate-level net list (1226) from the RTL design

description. As discussed above, the gate-level net list (1226) is related to synthesizable parts (combinational logic, registers, flip-flops).

Applicant respectfully submits that the gate-level net list of the Rostoker system is not equivalent to the object hierarchy of the claimed invention. In one embodiment of the invention discussed in the specification at page 17, lines 25-27, the object hierarchy is related to typical behavioral RT elements such as *signals, instructions and control states*. In contrast, the gate-level net list is a software schematic of combinational logic, registers and flip-flops, which are discrete hardware components and hardware circuits. That is, Rostoker at best transforms the RTL design description into a list of hardware related circuits. However, Rostoker does not disclose or teach transforming the behavioral register-transfer level design description to *an object hierarchy*.

Similarly, Rostoker does not teach or suggest creating an object that comprises a method capable of *transforming said object hierarchy into a second object hierarchy* that describes said target hardware component. Since Rostoker says nothing about transforming the object hierarchy into a second object hierarchy, the Rostoker reference cannot, and does not, teach or suggest creating an object that comprises a method capable of *transforming said object hierarchy into a second object hierarchy*. Thus, Rostoker does not suggest or teach all of the claim limitations of Claim 24.

In view of the above, neither Yeh, Rostoker, nor their combination teaches or suggests transforming the behavioral register-transfer level design description to an object hierarchy and creating an object that comprises a method capable of transforming said object hierarchy into a second object hierarchy recited in Claim 24. Absent such teaching or suggestion, no *prima facie* case has been established. Applicant respectfully requests withdrawal of the rejections.

Discussion of Patentability of Dependent Claims

Claims 25-26 and 28-29 depend from base Claim 24, and further define additional technical features of the present invention. In view of the patentability of their base claim, and in further view of their additional technical features, the dependent claims are patentable over the cited references.

CONCLUSION

In view of Applicant's amendments to the claims and the foregoing remarks, it is respectfully submitted that the present application is in condition for allowance. Should the Examiner have any remaining concerns which might prevent the prompt allowance of the application, the Examiner is respectfully invited to contact the undersigned at the telephone number appearing below.

Respectfully submitted,

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Dated: 10/31/03

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